6545 103658

SEARCH REQUEST FORM Scientific and Technical Information Center - EIC2800

Rev. 8/27/01 This is an experimental format -- Please give suggestions or comments to Jeff Harrison, CP4-9C18, 306-5429.

Date 9-10-03 Serial # 09/997,650 Priority Application Date 11-28-01

Your Name David Hogans Examiner # 79069

AU 2813 Phone 305-3361 Room cp4-4014

In what format would you like your results? Paper is the default. PAPER (DISK) EMAIL

If submitting more than one search, please prioritize in order of need.

The EIC searcher normally will contact you before beginning a prior art search. If you would like to sit with a searcher for an interactive search, please notify one of the searchers.

Where have you searched so far on this case? 09-11-03 A10:56 IN

Circle: (USPT) (DWPI) ~~EPO Abs~~ (JPO Abs) IBM TDB

Other: _____

What relevant art have you found so far? Please attach pertinent citations or Information Disclosure Statements. See Examiner search notes in center

What types of references would you like? Please checkmark:

Primary Refs ✓ Nonpatent Literature ✓ Other _____

Secondary Refs ___ Foreign Patents ✓

Teaching Refs ___

What is the topic, such as the **novelty**, motivation, utility, or other specific facets defining the desired **focus** of this search? Please include the concepts, synonyms, keywords, acronyms, registry numbers, definitions, structures, strategies, and anything else that helps to describe the topic. Please attach a copy of the abstract and pertinent claims.

Please search clm 9 & 6

novelty: doping a dielectric layer (insulator or oxide) w/ Indium between 1 & 15 mol. weight % and placing the layer over an active region (a transistor or active layer in a LED)

Staff Use Only	Type of Search	Vendors
Searcher: HARRISON 306-5429	Structure (#)	STN X
Searcher Phone:	Bibliographic X	Dialog X
Searcher Location: STIC-EIC2800, CP4-9C18	Litigation	Questel/Orbit
Date Searcher Picked Up: 9-24-03	Fulltext X	Lexis-Nexis
Date Completed: 9-24-03	Patent Family	WWW/Internet
Searcher Prep/Rev Time: 90	Other	Other
Online Time: 70		

STIC Search Report
EIC 2800

STIC Database Tracking Number: 103658

TO: David Hogans **Location: 4D14** **Art Unit: 2813** **9/24/03** **Case Serial Number: 09/997650**	**From: Jeff Harrison** **Location: STIC-EIC2800** **CP4-9C18** **Phone: 306-5429** **Email: harrison, jeff**

Search Notes

Examiner Hogans,

Attached are edited search results from the patent and NPL literature, mostly from Chemical Abstracts.

I tagged one abstract because it seemed to have an acceptable amount of Indium in a dielectric layer.

Based on this, if you have questions or would like a refocused search, please contact me.

Thanks,
Jeff

Jeff Harrison
Team Leader, STIC-EIC2800
CP4-9C18, 703-306-5429

FILE 'HCAPLUS' ENTERED AT 07:53:19 ON 24 SEP 2003
L1 1 S US2003100195/PN
L2 SEL PLU=ON L1 1- RN IC : 3 TERMS
L3 44816 S L2
L4 1 S L1 AND L3

FILE 'WPIX' ENTERED AT 07:54:33 ON 24 SEP 2003
L5 1 S US 2001-997650/PRN,AP

FILE 'REGISTRY' ENTERED AT 07:56:33 ON 24 SEP 2003
L6 1 S 7440-74-6/RN

FILE 'HCAPLUS' ENTERED AT 07:56:33 ON 24 SEP 2003
L7 37529 S L6
L8 2218 S L7(L)MOA/RL
L9 1905 S INDIUM DOPED
L10 4060 S L7(L)(IMPLANT##### OR IMPUR###### OR DOP####)
L11 11433 S INDIUM(2A)(CONCENTRATION OR WT OR WEIGHT
OR PERCENT OR ATOMIC OR DOP##### OR IMPUR#####)
L12 1049 S L8 AND (L9 OR L10 OR L11)
L13 1004 S L8 AND (L9 OR L10)
L14 696 S L11 AND L13
L15 228975 S "DIELECTRIC FILMS"/CT OR (OXIDE OR
INSULAT#### OR DIELECTRIC)(2A)(?LAYER? OR FILM)
L16 1582 S L7(L)(OXIDE OR INSULAT#### OR DIELECTRIC)
L17 75 S L14 AND L16

FILE 'REGISTRY' ENTERED AT 08:01:54 ON 24 SEP 2003
L18 3 S IN.O.SI/MF

FILE 'HCAPLUS' ENTERED AT 08:02:03 ON 24 SEP 2003
L19 5 S L18

FILE 'REGISTRY' ENTERED AT 08:02:35 ON 24 SEP 2003
L20 19406 S O.SI/MF OR O SI/ELF

FILE 'HCAPLUS' ENTERED AT 08:03:26 ON 24 SEP 2003
L21 434951 S L20
L22 973 S L21(L)INDIUM
L23 7148 S L21(L)DOP#####
L24 28 S L22 AND L23
L25 1 S L17 AND L22
L26 4 S L14 AND L22
L27 1185 S (L8 OR L9 OR L10 OR L11) AND L15
L28 28 S L27 AND L22
L29 92 S (L8 OR L9 OR L10 OR L11) AND L22
L30 5 S L29 AND L21(L)(INSULAT#### OR DIELECTRIC)
L31 7532 S INDIUM(3A)(15 OR 14 OR 13 OR 12 OR 11 OR 10 OR 9 OR 8 OR 7 OR 6 OR 5 OR 4 OR 3 OR 2 OR 1)
L32 976 S (L8 OR L9 OR L10 OR L11 OR L12 OR L13 OR L14 OR L15 OR L16) AND L31
L33 3 S L17 AND L31
L34 75 S (L22 OR L23 OR L24 OR L25 OR L26 OR L27 OR L28 OR L29) AND L31
L35 17 S L32 AND L22
L36 4 S L34 AND (INSULAT#### OR DIELECTRIC)(5A)INDIUM
L37 8 S L8 AND L34
L38 86 S L8 AND L32

FILE 'HCAPLUS' ENTERED AT 08:03:26 ON 24 SEP 2003
L39 12 S L38 AND (L21 OR DIELECTRIC OR INSULAT##### OR OXIDE(2A)(?LAYER? OR FILM))
L40 77 S (L24 OR L25 OR L26) OR L28 OR L30 OR L33 OR (L35 OR L36 OR L37) OR L39
L41 77 S L40 NOT (L19 OR L4)
L42 25 S L41 AND P/DT
L43 52 S L41 NOT L42
L44 6 S L43 AND PY>2001
L45 3181 S L8 OR L22
L46 256 S L45 AND (DIODE OR LED OR LIGHT(2A)EMIT##### OR EL OR ELECTROLUM?)
L47 180 S L45 AND ACTIVE
L48 78 S L45 AND ACTIVE(2A)(LAYER OR REGION OR FILM OR ZONE OR AREA)
L49 22 S L48 AND TRANSISTOR
L50 28 S L46 AND ACTIVE
L51 83 S L41 OR L19 OR L4
L52 48 S (L49 OR L50) NOT L51
L53 9 S L52 AND (DIELECTRIC OR INDIUM OR DOP#####)/ TI
L54 1 S L52 AND L7(L)(DIELECTRIC OR INSULAT#######)
L55 1602 S (DIELECTRIC OR INSULAT####### OR OXIDE)(3A)
ACTIVE AND ACTIVE(2A)(LAYER OR REGION OR FILM OR ZONE OR AREA)
L56 1 S L8 AND L55
L57 2 S INDIUM DOPED DIELECTRIC
L58 0 S INDIUM DOPED INSULAT#######
L59 4 S INDIUM DOPED OXIDE
L60 0 S INDIUM DOPED SIO
L61 0 S INDIUM DOPED SIO2
L62 0 S INDIUM DOPED(W)(SI OR SILICON)(W)(OXIDE OR DIOXIDE)
L63 1 S INDIUM DOPED(W)SILICA
L64 93 S L4 OR L19 OR L41 OR L53 OR L56
L65 94 S L64 OR L54
L66 6 S (L57 OR L58 OR L59 OR L60 OR L61 OR L62 OR L63) NOT L65
L67 SEL PLU=ON L66 1- RN : 17 TERMS
L68 1007162 S L67
L69 6 S L66 AND L68

FILE 'REGISTRY' ENTERED AT 08:40:57 ON 24 SEP 2003
L70 10554 S IN<15/MAC
L71 81 S L70 AND O/ELS,MAC
L72 17 S L71 AND SI/ELS,MAC
L73 826 S IN=15/MAC
L74 7 S L73 AND O/ELS,MAC
L75 2 S L74 AND SI/ELS,MAC
L76 19 S L72 OR L75

FILE 'HCAPLUS' ENTERED AT 08:42:26 ON 24 SEP 2003
L77 7 S L76

FILE 'REGISTRY' ENTERED AT 08:43:15 ON 24 SEP 2003
L78 86 S L71 OR L74

FILE 'HCAPLUS' ENTERED AT 08:43:45 ON 24 SEP 2003
L79 18 S L78 NOT L77
L80 25 S L77 OR L79
L81 0 S L80 AND DIELECTRIC
L82 2 S L80 AND INSULAT##########

FILE 'HCAPLUS, WPIX' ENTERED AT 15:19:12 ON 24 SEP 2003
L1 2 S US2001-0997650/PRN,AP
L2 SEL PLU=ON L1 1- IC MC : 6 TERMS
L3 48693 S L2
L4 0 S L3 AND INDIUM/CN(L) MOA/RL

FILE 'REGISTRY' ENTERED AT 15:20:12 ON 24 SEP 2003
L5 1 S INDIUM/CN
L6 33195 S IN/ELF,MF
L7 33192 S L6 AND IN/ELS
L8 180 S IN/MF

FILE 'HCAPLUS' ENTERED AT 15:22:38 ON 24 SEP 2003
L9 43961 S L8
L10 2341 S L9(L)MOA/RL
L11 33465 S DIELECTRIC FILM OR DIELECTRIC LAYER
L12 49 S L10 AND L11

File 2:INSPEC 1969-2003/Sep W2

*File 2: Alert feature enhanced for multiple files, duplicates removal, customized scheduling. See HELP ALERT.

Set	Items	Description
S1	2157	CI=IN DOP
S2	404	S1 AND CI=O
S3	68	S2 AND (DIELECTRIC?? OR INSULAT????? OR OXIDE()LAYER?? OR OXIDE()FILM??)
S4	1	S3 AND ACTIVE
S5	32	CI=(IN DOP(S)SI BIN(S)O BIN)(S)NE=2
S6	17	CI=(IN DOP(S)SI BIN(S)O BIN)(S)NE=3
S7	62	CI=(IN SS(S)SI SS(S)O SS)(S)NE=3
S8	144	S5:S7 OR S3
S9	43	S8 AND (DIELECTRIC?? OR INSULAT????? OR OXIDE)()(LAYER?? OR FILM??)
S10	43	S9 NOT S4

File 94:JICST-EPlus 1985-2003/Sep W3
(c)2003 Japan Science and Tech Corp(JST)

Set	Items	Description
S1	0	INDIUM()DOPED()DIELECTRIC??
S2	0	INDIUM()DOPED()INSULAT??????
S3	19	INDIUM()DOPED
S4	3	S3 AND (INSULAT???? OR DIELECTRIC???)

24sep03 14:06:01 User259284 Session D2398.3

File 2:INSPEC 1969-2003/Sep W2

*File 2: Alert feature enhanced for multiple files, duplicates removal, customized scheduling. See HELP ALERT.

Set	Items	Description
S1	518	INDIUM()DOPED OR INDIUM()DOPANT
S2	2157	CI=IN DOP
S3	254	1AND2
S4	33	S3 AND INSULAT??????????
S5	1	S3 AND DIELECTRIC??
S6	33	S4 NOT S5
S7	10	S6 AND (INSULAT????? OR DIELECTRIC??)/TI
S8	1670	DOP????(2N)(INSULAT???? OR DIELECTRIC????)
S9	7	6AND8

```
SYSTEM:OS  - DIALOG OneSearch
  File 348:EUROPEAN PATENTS  1978-2003/Sep W02
         (c) 2003 European Patent Office
  File 349:PCT FULLTEXT  1979-2002/UB=20030918,UT=20030911
         (c) 2003 WIPO/Univentio
  File 610:Business Wire  1999-2003/Sep 24
         (c) 2003 Business Wire.
*File 610: File 610 now contains data from 3/99 forward.
Archive data (1986-2/99) is available in File 810.
  File 613:PR Newswire  1999-2003/Sep 24
         (c) 2003 PR Newswire Association Inc
*File 613: File 613 now contains data from 5/99 forward.
Archive data (1987-4/99) is available in File 813.
  File 621:Gale Group New Prod.Annou.(R)  1985-2003/Sep 24
         (c) 2003 The Gale Group
  File 649:Gale Group Newswire ASAP(TM)  2003/Sep 22
         (c) 2003 The Gale Group
  File 810:Business Wire  1986-1999/Feb 28
         (c) 1999 Business Wire
  File 813:PR Newswire  1987-1999/Apr 30
         (c) 1999 PR Newswire Association Inc
  File   9:Business & Industry(R)  Jul/1994-2003/Sep 23
         (c) 2003 Resp. DB Svcs.
  File  16:Gale Group PROMT(R)  1990-2003/Sep 23
         (c) 2003 The Gale Group
*File  16: Alert feature enhanced for multiple files, duplicate
removal, customized scheduling. See HELP ALERT.
  File  47:Gale Group Magazine DB(TM)  1959-2003/Sep 23
         (c) 2003 The Gale group
  File  80:TGG Aerospace/Def.Mkts(R)  1986-2003/Sep 23
         (c) 2003 The Gale Group
  File  93:TableBase(R) Sep  1997-2003/Sep W2
         (c) 2003 Resp. DB Svcs.
  File 111:TGG Natl.Newspaper Index(SM)  1979-2003/Sep 22
         (c) 2003 The Gale Group
  File 112:UBM Industry News  1998-2003/Sep 24
         (c) 2003 United Business Media
  File 116:Brands & Their Companies  2003/Sep
         (c) 2003 Gale Research Inc.
  File 141:Readers Guide  1983-2003/Aug
         (c) 2003 The HW Wilson Co
  File 148:Gale Group Trade & Industry DB  1976-2003/Sep 24
         (c)2003 The Gale Group
*File 148: Alert feature enhanced for multiple files, duplicate
removal, customized scheduling. See HELP ALERT.
  File 149:TGG Health&Wellness DB(SM)  1976-2003/Sep W1
         (c) 2003 The Gale Group
  File 160:Gale Group PROMT(R)  1972-1989
         (c) 1999 The Gale Group
  File 177:Adv.& Agency Red Books:Advertisers  2003/Sep
         (c) 2003 Reed Elsevier Inc
  File 178:Adv.& Agency Red Books:Agencies  2003/Sep
         (c) 2003 Reed Elsevier Inc
  File 188:Health Devices Sourcebook  2002
         ECRI (A nonprofit agency)
  File 198:Health Devices Alerts(R)  1977-2003/Sep W3
         (c) 2003 ECRI-nonprft agncy
  File 211:Gale Group Newsearch(TM)  2003/Sep 24
         (c) 2003 The Gale Group
  File 233:Internet & Personal Comp. Abs.  1981-2003/Jul
         (c) 2003, EBSCO Pub.
  File 256:SoftBase:Reviews,Companies&Prods.  82-2003/Aug
         (c)2003 Info.Sources Inc
  File 275:Gale Group Computer DB(TM)  1983-2003/Sep 23
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        (c) 2003 The Gale Group
  File 481:DELPHES Eur Bus  95-2003/Sep W2
        (c) 2003 ACFCI & Chambre CommInd Paris
  File 482:Newsweek  2000-2003/Sep 13
        (c) 2003 Newsweek, Inc.
  File 484:Periodical Abs Plustext  1986-2003/Sep W3
        (c) 2003 ProQuest
*File 484: SELECT IMAGE AVAILABILITY FOR PROQUEST FILES
ENTER 'HELP PROQUEST' FOR MORE
  File 535:Thomas Register Online(R)  -2003/Q2
        (c) 2003 Thomas Publishing Co.
  File 571:Piers Exports(US Ports)  2003/Sep W3
        (c) 2003 Commonwealth Bus. Media
  File 573:Piers Imports(US Ports)  2003/Sep W3
        (c) 2003 Commonwealth Bus. Media
  File 583:Gale Group Globalbase(TM)  1986-2002/Dec 13
        (c) 2002 The Gale Group
*File 583: This file is no longer updating as of 12-13-2002.
  File 584:KOMPASS USA  2003/Jul
        (c) 2003 KOMPASS International
  File 585:KOMPASS Middle East/Africa/Mediterr  2003/Jul
        (c) 2003 KOMPASS Intl.
  File 586:KOMPASS Latin America  2003/Jul
        (c) 2003 KOMPASS International
  File 590:KOMPASS Western Europe  2003/Jun
        (c) 2003 KOMPASS International
  File 592:KOMPASS Asia/Pacific  2003/Jul
        (c) 2003 KOMPASS International
  File 593:KOMPASS Central/Eastern Europe  2003/Jul
        (c) 2003 KOMPASS Intl.
  File 609:Bridge World Markets  2000-2001/Oct 01
        (c) 2001 Bridge
*File 609: This file is closed.
  File 636:Gale Group Newsletter DB(TM)  1987-2003/Sep 23
        (c) 2003 The Gale Group
  File 646:Consumer Reports  1982-2003/Sep
        (c) 2003 Consumer Union
  File 647:CMP  Computer Fulltext  1988-2003/Aug W5
        (c) 2003 CMP Media, LLC


Set     Items   Description
S1          0   INDIUM()DOPED()DIELECTRIC??
S2          0   INDIUM()IMPLANTED()DIELECTRIC??
S3        230   INDIUM()DOPED
S4         18   INDIUM()IMPLANT???????
S5        413   INDIUM()(DOPANT?? OR DOPE?? OR DOPING)
S6          5   INDIUM()IMPURITY
S7         47   INDIUM()IONS
S8         32   INDIUM()ION
S9         87   INDIUM()ATOM? ?
S10       724   INDIUM(6N)(DIELECTRIC?? OR INSULAT?????)
S11       582   S1:S9
S12        14   10AND11
S13        14   RD S12 (unique items)
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SYSTEM:OS  - DIALOG OneSearch
  File   2:INSPEC  1969-2003/Sep W2
         (c) 2003 Institution of Electrical Engineers
*File   2: Alert feature enhanced for multiple files, duplicates
removal, customized scheduling. See HELP ALERT.
  File   6:NTIS  1964-2003/Sep W3
         (c) 2003 NTIS, Intl Cpyrght All Rights Res
  File   8:Ei Compendex(R)  1970-2003/Sep W2
         (c) 2003 Elsevier Eng.  Info. Inc.
  File  25:Weldasearch  1966-2002/Mar
         (c) 2003 TWI Ltd
  File  31:World Surface Coatings Abs  1976-2003/Aug
         (c) 2003 Paint Research Assn.
  File  34:SciSearch(R) Cited Ref Sci  1990-2003/Sep W2
         (c) 2003 Inst for Sci Info
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         (c) 2003 ProQuest Info&Learning
  File  63:Transport Res(TRIS)  1970-2003/Aug
         (c) fmt only 2003 Dialog Corp.
  File  65:Inside Conferences  1993-2003/Sep W3
         (c) 2003 BLDSC all rts. reserv.
  File  81:MIRA - Motor Industry Research  2001-2003/Jul
         (c) 2003 MIRA Ltd.
  File  87:TULSA (Petroleum Abs)  1965-2003/Sep W4
         (c)2003 The University of Tulsa
  File  94:JICST-EPlus  1985-2003/Sep W3
         (c)2003 Japan Science and Tech Corp(JST)
  File  95:TEME-Technology & Management  1989-2003/Sep W1
         (c) 2003 FIZ TECHNIK
  File  96:FLUIDEX  1972-2003/Sep
         (c) 2003 Elsevier Science Ltd.
  File  99:Wilson Appl. Sci & Tech Abs  1983-2003/Aug
         (c) 2003 The HW Wilson Co.
  File 103:Energy SciTec  1974-2003/Sep B1
         (c) 2003 Contains copyrighted material
*File 103: For access restrictions see Help Restrict.
  File 118:ICONDA-Intl Construction  1976-2003/Aug
         (c) 2003 Fraunhofer-IRB
  File 144:Pascal  1973-2003/Sep W2
         (c) 2003 INIST/CNRS
  File 239:Mathsci  1940-2003/Nov
         (c) 2003 American Mathematical Society
  File 240:PAPERCHEM  1967-2003/Sep W3
         (c) 2003 Elsevier Eng. Info. Inc.
  File 248:PIRA  1975-2003/Sep W3
         (c) 2003 Pira International
*File 248: Changes have been made to Subject Headings and Codes as of
July 2002. See Help Codes248 for a complete list of Subject Headings.
  File 315:ChemEng & Biotec Abs  1970-2003/Aug
         (c) 2003 DECHEMA
  File 323:RAPRA Rubber & Plastics  1972-2003/Sep
         (c) 2003 RAPRA Technology Ltd
*File 323: Alert feature enhanced for multiple files, duplicate
removal, customized scheduling.  See HELP ALERT.
  File 434:SciSearch(R) Cited Ref Sci  1974-1989/Dec
         (c) 1998 Inst for Sci Info
  File 350:Derwent WPIX  1963-2003/UD,UM &UP=200361
         (c) 2003  Thomson Derwent
  File 347:JAPIO  Oct 1976-2003/May(Updated 030902)
         (c) 2003 JPO & JAPIO
*File 347: JAPIO data problems with year 2000 records are now fixed.
Alerts have been run.  See HELP NEWS 347 for details.
```

Set	Items	Description
S1	1	INDIUM()DOPED()DIELECTRIC
S2	0	INDIUM()DOPED()INSULAT????
S3	1	INDIUM()DOPED()OXIDE??
S4	0	INDIUM()DOPED()SILICA
S5	1	INDIUM()DOPED()(SI OR SILICON)()(OXIDE OR DIOXIDE)
S6	2	S1 OR S3 OR S5

10/9/11
DIALOG(R)File 2:INSPEC

5757011 INSPEC Abstract Number: A9801-7865-033, B9801-2520D-019
Title: Optical and electrical properties of doped zinc **oxide films** prepared by ac reactive magnetron sputtering
Author(s): Szyszka, B.; Jager, S.
Author Affiliation: Fraunhofer Inst. for Surface Eng. & Thin Films, Braunschweig, Germany
Journal: Journal of Non-Crystalline Solids Conference Title: J. Non-Cryst. Solids (Netherlands) vol.218 p.74-80
Publisher: Elsevier,
Publication Date: Sept. 1997 Country of Publication: Netherlands
CODEN: JNCSBJ ISSN: 0022-3093
SICI: 0022-3093(199709)218L.74:OEPD;1-7
Material Identity Number: J120-97019
U.S. Copyright Clearance Center Code: 0022-3093/97/$17.00
Conference Title: Coating on Glass. First International Conference. Advanced Technologies and Future Trends for High Volume and/or Large Areas
Conference Sponsor: Asahi Glass Co.; The BOC Group; Cardinal IG; Leybold Mater. GmbH; Leybold Syst. GmbH; et al
Conference Date: 27-31 Oct. 1997 Conference Location: Saabrucken, Germany
Document Number: S0022-3093(97)00288-3
Language: English Document Type: Conference Paper (PA); Journal Paper (JP)
Treatment: Experimental (X)
Abstract: Aluminum-doped and indium-doped zinc **oxide films** have been prepared by reactive ac magnetron sputtering (twin-cathode arrangement with ac plasma excitation at frequency of 40 kHz) from metallic targets with different dopant concentrations at substrate temperature of about 573 K. The optical, electrical and structural properties of the sputtered ZnO:Al and ZnO:In thin films have been investigated by optical spectroscopy (UV-IR), X-ray diffraction, Hall-mobility and conductivity measurements. For aluminum-doped ZnO films a minimum resistivity of 4.0*10/sup -4/ Omega cm at high transparency (larger than 89% at film thickness of 530 nm) has been obtained at Al concentration in the target material of 1.2 wt%. Higher resistivity of 8.7*10/sup -4/ Omega cm (85% transmission at film thickness of 400 nm) has been observed for indium-doped zinc **oxide films** at dopant concentration of about 2 wt% In in the target material. (17 Refs)
Subfile: A B
Chemical Indexing:
ZnO:In ss - In ss - Zn ss - O ss - ZnO bin - Zn bin - O bin - In el - **In dop** (Elements - 2,1,3)

No active region

10/9/12
DIALOG(R)File 2:INSPEC

5642920 INSPEC Abstract Number: A9717-6855-075, B9709-2520E-002
Title: Characterization of indium-doped zinc **oxide films** deposited by pyrolytic spray with different indium compounds as dopants
Author(s): Gomez, H.; Maldonado, A.; Asomoza, R.; Zironi, E.P.; Canetas-Ortega, J.; Palacios-Gomez, J.
Author Affiliation: Centro de Investigacion y de Estudios Avanzados, Inst. Politecnico Nacional, Mexico City, Mexico
Journal: Thin Solid Films vol.293, no.1-2 p.117-23
Publisher: Elsevier,
Publication Date: 30 Jan. 1997 Country of Publication: Switzerland
CODEN: THSFAP ISSN: 0040-6090
SICI: 0040-6090(19970130)293:1/2L.117:CIDZ;1-J
Material Identity Number: T070-97008
U.S. Copyright Clearance Center Code: 0040-6090/97/$17.00
Document Number: S0040-6090(96)09001-3
Language: English Document Type: Journal Paper (JP)
Treatment: Experimental (X)
Abstract: The results of a systematic study of the electrical, optical, structural and surface properties of thin ZnO:In films are presented. The films were deposited by the spray pyrolysis technique. The spraying solution was zinc acetate diluted in methanol and the indium doping was achieved by adding indium acetate, indium nitrate and indium sulfate at different concentrations up to [In]/[Zn]=3 at%. The films grown at low temperature show regular and uniformly smooth surfaces with no texturization. Films grown at high temperature show rough surfaces. All the films are polycrystalline and grow with a (101) preferred orientation. The electrical resistivity measured at room temperature shows a minima in all cases as a function of the substrate temperature. The lowest value, rho =2*10/sup -3/ Omega cm, was obtained by doping with indium acetate at a [In]/[Zn]=3 at% concentration. For films about 0.6 mu m thick the average transmittance was better than 85%. A shift in the energy gap due to a variation in the carrier concentration was observed. This shift is explained with a model in which the Burstein-Moss effect and the electron-electron exchange interaction are considered. (29 Refs)
Subfile: A B
Chemical Indexing:
ZnO:In ss - In ss - Zn ss - O ss - ZnO bin - Zn bin - O bin - In el - **In dop** (Elements - 2,1,3)

No active

10/9/8
DIALOG(R)File 2:INSPEC

5844385 INSPEC Abstract Number: A9807-4270-009, B9804-4120-006
Title: Optical recording in Ga and In-doped zinc oxide thin films grown by radio-frequency magnetron sputtering
Author(s): Matsushita, T.; Suzuki, A.; Toda, S.; Aoki, T.; Okuda, M.
Author Affiliation: Dept. of Electr. Eng. & Electron., Osaka Sangyo Univ., Japan
Journal: Japanese Journal of Applied Physics, Part 2 (Letters) vol.37, no.1A-B p.L50-2
Publisher: Publication Office, Japanese Journal Appl. Phys,
Publication Date: 15 Jan. 1998 Country of Publication: Japan
CODEN: JAPLD8 ISSN: 0021-4922
SICI: 0021-4922(19980115)37:1ABL.150:ORDZ;1-K
Material Identity Number: C580-98002
Language: English Document Type: Journal Paper (JP)
Treatment: Applications (A); Experimental (X)
Abstract: Thin films of Zn-Ga-In oxide have been deposited on glass substrate at room temperature by RF magnetron sputtering with three targets of Zn, ZnO doped with 7 wt% Ga/sub 2/O/sub 3/ and ZnO doped with 7 wt% In/sub 2/O/sub 3/. In the **oxide films** prepared by this method, the difference in the transmittance, Delta T, between the annealed state (350 degrees C*30 min) and the as-deposited state was 41% at 380 nm, 61% at 390 nm and 72% at 400 nm. The ability to record on these **oxide films** without a protection layer, using SHG of a Nd:YAG laser (lambda =532 nm, 6 ns, 69 mW/ mu m/sup 2/) was confirmed. (14 Refs)
Subfile: A B

No active

L41 ANSWER 28 OF 77 HCAPLUS COPYRIGHT 2003 ACS on STN
AN 1997:507521 HCAPLUS
DN 127:192990
TI Highly textured ZnO thin films and SnO2/ZnO bilayer films prepared by the pyrosol process
AU Song, Jinsoo; Lee, Changhyun; Lim, Koengsu; Yoon, Kyunghoon; Yu, Kwonjong
CS Korea Institute of Energy Research, Taejon, S. Korea
SO Conference Record of the IEEE Photovoltaic Specialists Conference (1996), 25th, 1141-1144
CODEN: CRCNDP; ISSN: 0160-8371
PB Institute of Electrical and Electronics Engineers
DT Journal
LA English
CC 52-2 (Electrochemical, Radiational, and Thermal Energy Technology)
AB ZnO:In films have been prepd. on heated Corning 7059 glass by pyrosol spray method. Indium improves the cond. as an n-type dopant and stimulates grain growth. For films grown at 400.degree., resistivity of ZnO films decreased from 1.3.times.10-2 .OMEGA.cm to 3.5.times.10-3 .OMEGA.cm by **doping 1 wt% indium**. Furthermore, ZnO:In films grown at higher temp. revealed larger grain sizes and a higher texturization compared to undoped films. A highly textured ZnO:In films with resistivity of 2.5.times.10-3 .OMEGA.cm, total transmittance of 80% was made at the substrate temp. of 475.degree., and was milky looking. ZnO:In films did not degrade under hydrogen plasma, and was applied as a protection barrier against hydrogen plasma and light scattering layer in SnO2/ZnO bilayer films. Bilayer films have resistivity of 8.8.times.10-4 .OMEGA.cm and total transmittance of 84% at 550 nm, and was proved to have an excellent hydrogen plasma durability.
IT **7440-74-6, Indium**, uses
RL: **MOA (Modifier or additive use)**; USES (Uses)
(ZnO **doped** with; highly textured ZnO thin films and SnO2/ZnO bilayer films prepd. by the pyrosol process)
RN 7440-74-6 HCAPLUS
CN Indium (8CI, 9CI) (CA INDEX NAME)

In

No active

10/9/17
DIALOG(R)File 2:INSPEC

5187968 INSPEC Abstract Number: A9606-6855-025
Title: Zinc oxide thin films by the spray pyrolysis method
Author(s): Krunks, M.; Mellikov, E.
Author Affiliation: Inst. of Mater. Tech., Tallinn Tech. Univ., Estonia
Journal: Thin Solid Films Conference Title: Thin Solid Films (Switzerland) vol.270, no.1-2 p.33-6
Publisher: Elsevier,
Publication Date: 1 Dec. 1995 Country of Publication: Switzerland
CODEN: THSFAP ISSN: 0040-6090
SICI: 0040-6090(19951201)270:1/2L.33:ZOTF;1-Q
Material Identity Number: T070-96001
U.S. Copyright Clearance Center Code: 0040-6090/95/$09.50
Conference Title: 22nd International Conference on Metallurgical Coating and Thin Films
Conference Date: 24-28 April 1995 Conference Location: San Diego, CA, USA
Language: English Document Type: Conference Paper (PA); Journal Paper (JP)
Treatment: Experimental (X)
Abstract: Undoped and In-doped ZnO thin films have been prepared on glass substrates from solutions of Zn(CH/sub 3/CO/sub 2/)/sub 2/.2H/sub 2/O in a mixture of deionized water and isopropyl alcohol by spray pyrolysis. Their optical, morphological and structural qualities have been studied and the effect of the preparation conditions discussed. It was shown that the main factors determining the parameters of ZnO films are the growth temperature and the indium concentration. The growth temperatures of 625-675 K, indium doping levels of 1-1.5 at.% and precursor concentrations of 0.1-0.2 mol 1/sup -1/ are preferable to achieve ZnO films with optical and structural qualities as required for solar cell applications. (10 Refs)
Subfile: A
Descriptors: indium; infrared spectra; pyrolysis; scanning electron
Chemical Indexing:
ZnO:In ss - In ss - Zn ss - O ss - ZnO bin - Zn bin - O bin - In el - **In dop** (Elements - 2,1,3)

L12 ANSWER 9 OF 49 HCAPLUS COPYRIGHT 2003 ACS on STN
AN 2003:376320 HCAPLUS
DN 138:361359
TI Photoelectric conversion element and method of manufacturing the same
IN Nagashima, Tomonori; Okumura, Kenichi
PA Toyota Jidosha Kabushiki Kaisha, Japan
SO U.S. Pat. Appl. Publ., 22 pp.
CODEN: USXXCO
DT Patent
LA English
IC ICM H01L021-338
NCL 438184000
CC 76-3 (Electric Phenomena)
Section cross-reference(s): 52

11/13/01 priority

FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 2003092226	A1	20030515	US 2002-291638	20021112
	JP 2003152207	A2	20030523	JP 2001-347808	20011113
PRAI	JP 2001-347808	A	20011113		

AB In a back-surface electrode type photoelec. conversion element having electrodes and semiconductor layers for collecting carriers disposed only on a back surface side of a semiconductor substrate, a semiconductor thin film that is larger in band gap than the semiconductor substrate and that contains an element causing a cond. identical to or different from a cond. of the semiconductor substrate is provided on a light-receiving surface side of the semiconductor substrate, and a diffusion layer is formed on a surface of the semiconductor substrate. Alternatively, 95% or more of light beams having a wavelength of anywhere from 800 nm to 2000 nm are caused to penetrate the light-receiving surface side of the semiconductor substrate, and an insulative thin film contg. an element causing a cond. identical to or different from the cond. of the semiconductor substrate is provided so as to form a diffusion layer on the surface of the semiconductor substrate through diffusion of the element.

IT **Dielectric films**
Electric conductivity
Electric insulators
IT **7440-74-6**, Indium, uses
RL: **MOA (Modifier or additive use)**; USES (Uses)
(photoelec. conversion element and manuf. of same)
RN 7440-74-6 HCAPLUS
CN Indium (8CI, 9CI) (CA INDEX NAME)

In

L12 ANSWER 10 OF 49 HCAPLUS COPYRIGHT 2003 ACS on STN
AN 2003:319222 HCAPLUS
DN 138:330090
TI Method for establishing contact between interconnection and substrate in an integrated circuit
IN Reber, Douglas M.
PA USA
SO U.S. Pat. Appl. Publ., 7 pp.
CODEN: USXXCO
DT Patent
LA English
IC ICM H01L023-48
NCL 257773000; 257781000
CC 76-3 (Electric Phenomena)
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 2003075806	A1	20030424	US 2001-986232	20011022
	US 6555915	B2	20030429		
	WO 2003036702	A2	20030501	WO 2002-US30337	20020927

AB This invention relates to integrated circuits and more particularly to making contact between interconnect and substrate. A contact between a source/drain and a gate is made by making a selected portion of the gate dielec. conductive by an implant into that selected portion of the gate dielec. The gate material is in a layer over the entire integrated circuit. Areas where gates are to connect to source/drains are identified and the gate dielec. at those identified locations is implanted to make it conductive. The source/drains are formed so that they extend under these areas of conductive gate dielec. so that at these locations the implanted gate dielec. shorts the gate to the source/drain. This saves area on the integrated circuit, reduces the need for interconnect layers, and avoids the problems assocd. with depositing and etching polysilicon on an exposed Si substrate.

IT **Dielectric films**
Electric contacts

IT **7440-74-6**, Indium, uses
RL: DEV (Device component use); **MOA (Modifier or additive use)**; USES (Uses)
(silica doped with; method for establishing contact between interconnection and substrate in an integrated circuit)

RN 7440-74-6 HCAPLUS
CN Indium (8CI, 9CI) (CA INDEX NAME)

In

10/22/01 priority

no In doping levels

L12 ANSWER 11 OF 49 HCAPLUS COPYRIGHT 2003 ACS on STN
AN 2003:255146 HCAPLUS
DN 138:264142
TI Barrier-to-seed layer alloying in integrated circuit interconnects
IN Woo, Christy Mei-Chu; Wang, Pin-Chin Connie; Bernard, Joffre F.
PA Advanced Micro Devices, Inc., USA
SO U.S., 7 pp.
CODEN: USXXAM
DT Patent
LA English
IC ICM H01L023-48
NCL 257751000; 257750000; 257758000
CC 76-3 (Electric Phenomena)
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6541860	B1	20030401	US 2001-875457	20010605
PRAI	US 2001-875457		20010605		

AB The present invention relates generally to semiconductor technol. and more specifically to alloying the material at the barrier layer to seed layer interface in integrated circuit interconnects. An integrated circuit and a method for manuf. thereof are provided having a semiconductor substrate with a semiconductor device. A device **dielec. layer** is formed on the semiconductor substrate. An opening is formed in the **dielec. layer**. A barrier layer with an alloying element is deposited to line the opening in the **dielec. layer**. A conductor core is deposited on the barrier layer to fill the opening and connect to the semiconductor device. The conductor core is annealed causing migration of the alloy element into the conductor core.

IT Alloying
Annealing
Dielectric films
Diffusion barrier
Electric insulators

IT **7440-74-6**, Indium, uses
RL: DEV (Device component use); **MOA (Modifier or additive use)**;
USES (Uses)
(alloy element; barrier-to-seed layer alloying in integrated circuit interconnects)

RN 7440-74-6 HCAPLUS
CN Indium (8CI, 9CI) (CA INDEX NAME)

In

L12 ANSWER 12 OF 49 HCAPLUS COPYRIGHT 2003 ACS on STN
AN 2003:201575 HCAPLUS
DN 138:213744
TI Method for fabricating a metal-insulator-semiconductor device
IN Noda, Taiji
PA Matsushita Electric Industrial Co., Ltd., Japan
SO Eur. Pat. Appl., 15 pp.
CODEN: EPXXDW
DT Patent
LA English
IC ICM H01L021-265
ICS H01L021-324; H01L021-336; H01L029-78
CC 76-3 (Electric Phenomena)
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI EP 1291905	A2	20030312	EP 2002-19813	20020905
R: AT, BE, CH, DE, DK, ES, FR, GB, GR, IT, LI, LU, NL, SE, MC, PT, IE, SI, LT, LV, FI, RO, MK, CY, AL, TR, BG, CZ, EE, SK				
JP 2003086791	A2	20030320	JP 2001-271330	20010907
US 2003049917	A1	20030313	US 2002-235830	20020906
PRAI JP 2001-271330	A	20010907		

AB The present invention relates to MIS-semiconductor-device fabrication methods for attaining further reduced dimension while enabling high-speed operation with low power consumption. As impurity ions for forming a channel, heavy ions are implanted multiple times at a dose such that no dislocation-loop defect layer is caused to be formed, and an annealing process is performed after each ion implantation process has been carried out, thereby forming a heavily doped channel layer having a steep retro-grade impurity profile.

IT **7440-74-6**, Indium, uses
RL: DEV (Device component use); **MOA (Modifier or additive use)**;
USES (Uses)
(method for fabricating a metal-insulator-semiconductor device)
RN 7440-74-6 HCAPLUS
CN Indium (8CI, 9CI) (CA INDEX NAME)

In

L12 ANSWER 14 OF 49 HCAPLUS COPYRIGHT 2003 ACS on STN
AN 2003:71818 HCAPLUS
DN 138:116410
TI SOI device with structure for enhancing carrier recombination and fabrication of same
IN Ju, Dong-Hyuk; En, William G.; Krishnan, Srinath; An, Xilin Judy
PA Advanced Micro Devices, Inc., USA
SO U.S., 7 pp.
CODEN: USXXAM
DT Patent
LA English
IC ICM H01L021-20
NCL 257059000
CC 76-3 (Electric Phenomena)
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6512244	B1	20030128	US 2001-850392	20010507
PRAI	US 2001-850392		20010507		

AB The silicon-on-insulator (SOI) device includes an SOI wafer including an active layer, a substrate and a buried insulation layer disposed therebetween. The active layer includes an abrupt region disposed along a lower portion of the active layer, the abrupt region having the same P or N doping type as a doping type of a body region.

IT **Dielectric films**
Doping
Electric current carriers
Electric insulators
IT **7440-74-6**, Indium, uses
RL: **MOA (Modifier or additive use)**; USES (Uses)
(SOI device with structure for enhancing carrier recombination and fabrication of same)
RN 7440-74-6 HCAPLUS
CN Indium (8CI, 9CI) (CA INDEX NAME)

In

No concentrations
& In layer not formed
over active

L12 ANSWER 15 OF 49 HCAPLUS COPYRIGHT 2003 ACS on STN
AN 2003:53557 HCAPLUS
DN 138:99491
TI Design of SOI devices with self-aligned floating body control
IN En, William George; Krishnan, Srinath; An, Judy Xilin
PA Advanced Micro Devices, Inc., USA
SO U.S., 10 pp.
CODEN: USXXAM
DT Patent
LA English
IC ICM H01L027-01
NCL 257349000; 257347000; 257348000; 257376000
CC 76-3 (Electric Phenomena)
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI US 6509613	B1	20030121	US 2001-849494	20010504
PRAI US 2001-849494		20010504		

AB The invention relates to the design of semiconductor-on-insulator (SOI) devices with self-aligned floating body control through a leakage enhanced buried oxide. A SOI device is formed on an SOI structure with a buried oxide (BOX) layer and an active region disposed on the BOX layer having active regions defined by isolation trenches and the BOX layer. The SOI device includes a gate formed over one of the active regions. The gate defines a channel interposed between a source and a drain formed within one of the active regions. The SOI device includes a leakage enhanced region within the BOX layer defined by the gate.

IT **7440-74-6**, Indium, processes
RL: **MOA (Modifier or additive use)**; PEP (Physical, engineering or chemical process); PYP (Physical process); PROC (Process); USES (Uses)
(dopant; design of SOI devices with self-aligned floating body control)
RN 7440-74-6 HCAPLUS
CN Indium (8CI, 9CI) (CA INDEX NAME)

In

No formed over active region
No concentrations

L41 ANSWER 7 OF 77 HCAPLUS COPYRIGHT 2003 ACS on STN
AN 2003:1256 HCAPLUS
DN 138:32006
TI Design of an n-type MOS device with an indium pocket implant region to reduce short channel effects
IN Wang, Howard Chih-hao; Lu, Su-yu; Chiang, Mu-chi; Diaz, Carlos H.
PA Taiwan Semiconductor Manufacturing Company, Taiwan
SO U.S., 8 pp.
CODEN: USXXAM
DT Patent
LA English
IC ICM H01L021-425
NCL 438514000; 438513000; 438525000; 438528000; 438305000; 438286000
CC 76-3 (Electric Phenomena)
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6500739	B1	20021231	US 2001-880260	20010614
PRAI	US 2001-880260		20010614		

AB The invention relates to the design of an n-type metal-oxide-semiconductor (NMOS) device with a narrow channel region and an indium pocket implant region to reduce short channel effects (SCE) such as punch-through leakage and voltage roll-off. An indium pocket implant region is formed in the area of a p-type semiconductor to be used to accommodate an n-type source/drain region. An ion implantation procedure is used to place antimony ions in the indium pocket implant region. The presence of antimony ions limits the broadening of the indium pocket implant profile during subsequent anneal procedures, which are used to activate the implanted ions. Formation of an implanted lightly doped n-type source/drain region, insulator spacers on the sides of a gate structure, and formation of a heavily doped n-type source/drain region complete the process sequence used to form the NMOS transfer gate transistor.

IT Annealing
Dielectric films
Doping
Ion implantation
IT **7440-74-6, Indium,** processes
RL: **MOA (Modifier or additive use)**; PEP (Physical, engineering or chemical process); PYP (Physical process); PROC (Process); USES (Uses)
(**dopant;** design of an n-type MOS device with an indium pocket **implant** region to reduce short channel effects)
RN 7440-74-6 HCAPLUS
CN Indium (8CI, 9CI) (CA INDEX NAME)

In

IT **7631-86-9,** Silica, uses
RL: DEV (Device component use); USES (Uses)
(**insulator;** design of an n-type MOS device with an **indium** pocket implant region to reduce short channel effects)
RN 7631-86-9 HCAPLUS
CN Silica (6CI, 7CI, 8CI, 9CI) (CA INDEX NAME)

O=Si=O

No form in dielectric
No conc.

L12 ANSWER 20 OF 49 HCAPLUS COPYRIGHT 2003 ACS on STN
AN 2002:928177 HCAPLUS
DN 138:10424
TI Method for forming nitride read only memory with indium pocket region
IN Chen, Chia-Hsing
PA Taiwan
SO U.S. Pat. Appl. Publ., 9 pp.
CODEN: USXXCO
DT Patent
LA English
IC ICM H01L021-425
NCL 438514000; 438517000
CC 76-3 (Electric Phenomena)
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 2002182829	A1	20021205	US 2001-870530	20010531
PRAI	US 2001-870530		20010531		

AB A method for the fabrication of a nitride ROM of high yield and quality is claimed. First of all, a P-type semiconductor substrate is provided. Then an oxide-nitride-oxide layer is formed on the P-type semiconductor substrate. Afterward, a photoresist layer is formed on the oxide-nitride-oxide layer, and it is defined to form a plurality of photoresist regions on the oxide-nitride-oxide layers. The oxide-nitride-oxide layer is then etched to form a plurality of nitride read only memory cells. Subsequently, perform a pocketed implantation with In ions to form a plurality of pocket dopant regions under a plurality of nitride read only memory cells, resp. Next, perform a N-type ion-implanting process to form a plurality of ion-implanting regions in the P-type semiconductor substrate between a plurality of nitride read only memory cells. Finally, a plurality photoresist regions are removed to form an nitride read only memory.

IT **Dielectric films**
Doping
Etching
Ion implantation
IT **7440-74-6**, Indium, uses
RL: **MOA (Modifier or additive use)**; USES (Uses)
(forming nitride read only memory with indium pocket region)
RN 7440-74-6 HCAPLUS
CN Indium (8CI, 9CI) (CA INDEX NAME)

In

No active ingr.

No

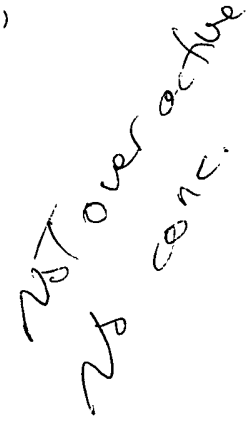
L12 ANSWER 21 OF 49 HCAPLUS COPYRIGHT 2003 ACS on STN
AN 2002:921870 HCAPLUS
DN 138:10574
TI Process of diffusing and activating dopants in dielectric or semiconductor substrates using electron beam irradiation
IN Ross, Matthew F.; Hannes, Charles; Livesay, William R.
PA Electron Vision Corporation, USA
SO U.S., 9 pp.
CODEN: USXXAM
DT Patent
LA English
IC ICM H01L021-26
NCL 438535000; 438795000; 438798000
CC 76-12 (Electric Phenomena)
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6489225	B1	20021203	US 2000-590066	20000608
	US 2003008481	A1	20030109	US 2002-211854	20020802
PRAI	US 1999-138740P	P	19990611		
	US 2000-590066	A3	20000608		

AB The invention relates to the use of electron beam irradn. to distribute and activate an n-type or p-type dopant following its application to a dielec. or semiconductor substrate. A dopant is introduced into a dielec. or semiconductor substrate. The substrate is then subjected to sufficient electron beam irradn. to distribute and activate the dopant in the substrate, where the electron beam energy level is 0.5-15 keV and the beam current is 1-150 mA.

IT **7440-74-6,** Indium, processes
RL: **MOA (Modifier or additive use)**; PEP (Physical, engineering or chemical process); PYP (Physical process); PROC (Process); USES (Uses)
(dopant; process of diffusing and activating dopants in dielec. or semiconductor substrates using electron beam irradn.)
RN 7440-74-6 HCAPLUS
CN Indium (8CI, 9CI) (CA INDEX NAME)

In



L53 ANSWER 1 OF 9 HCAPLUS COPYRIGHT 2003 ACS on STN
AN 2002:889240 HCAPLUS
DN 137:378676
TI Design and fabrication of a semiconductor device using MOS **transistors** with **indium-doped** pocket regions
IN Wada, Hajime; Okabe, Kenichi; Watanabe, Kou
PA Fujitsu Limtied, Japan
SO U.S., 15 pp.
CODEN: USXXAM
DT Patent
LA English
IC ICM H01L029-76
ICS H01L029-94; H01L031-062; H01L031-113; H01L031-119
NCL 257397000
CC 76-3 (Electric Phenomena)
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6483155	B1	20021119	US 2002-46978	20020117
	JP 2003017578	A2	20030117	JP 2001-198594	20010629
	CN 1393935	A	20030129	CN 2002-106726	20020304
	US 2003030112	A1	20030213	US 2002-266689	20021009
PRAI	JP 2001-198594	A	20010629		
	US 2002-46978	A3	20020117		

AB The invention relates to the design of a semiconductor device contg. an indium-doped MOS **transistor** in which the leak current is suppressed by performing an annealing step after the ion implantation. A semiconductor device has (i) first and second **active regions** defined on the principal surface of a silicon substrate; (ii) a first n-channel MOS **transistor** formed in an **active region** having extension regions, having pocket regions lying deeper than the extension regions, and being doped with indium; and (iii) a second n-channel MOS **transistor** formed in a sep. **active region** having extension regions, having pocket regions lying deeper than the extension regions, and being doped with indium at a concn. lower than that of the first **transistor**. Boron ions may also be implanted into the pocket regions of the second **transistor**.

IT Electric insulators
(isolation; design and fabrication of a semiconductor device using MOS **transistors** with indium-doped pocket regions)

IT **7440-74-6**, Indium, processes
RL: **MOA (Modifier or additive use)**; PEP (Physical, engineering or chemical process); PYP (Physical process); PROC (Process); USES (Uses)
(dopant; design and fabrication of a semiconductor device using MOS **transistors** with indium-doped pocket regions)

RN 7440-74-6 HCAPLUS
CN Indium (8CI, 9CI) (CA INDEX NAME)

In

Not in dielec. over active region

L12 ANSWER 23 OF 49 HCAPLUS COPYRIGHT 2003 ACS on STN
AN 2002:845520 HCAPLUS
DN 137:331983
TI Transistor with shaped gate electrode and method of fabrication
IN Taylor, William J., Jr.; Samavedam, Srikanth B.; Cave, Nigel
PA Motorola, Inc., USA
SO U.S., 10 pp.
CODEN: USXXAM
DT Patent
LA English
IC ICM H01L021-311
ICS H01L021-461
NCL 438197000
CC 76-3 (Electric Phenomena)
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6475841	B1	20021105	US 2000-584963	20000602
PRAI	US 2000-584963		20000602		

AB A transistor structure includes a retrograde gate structure that is narrower at the end that interfaces with the gate dielec. than it is at the opposite end and method for manuf. of such a structure. The retrograde gate structure is formed by depositing a layer of gate material that has varying compn. in the vertical direction. The differentiation in compn. causes varying lateral etch rate characteristics along the vertical direction of the gate structure such that increased etching of the gate material occurs near the interface with the gate **dielec.** **layer.**

IT **7440-74-6**, Indium, uses
RL: **MOA (Modifier or additive use)**; USES (Uses)
(transistor with shaped gate electrode and method of fabrication using)
RN 7440-74-6 HCAPLUS
CN Indium (8CI, 9CI) (CA INDEX NAME)

In

L53 ANSWER 2 OF 9 HCAPLUS COPYRIGHT 2003 ACS on STN
AN 2002:384958 HCAPLUS
DN 136:378477
TI Method of selectively controlling contact resistance of **transistors** by controlling **dopant** concentration and silicide thickness
IN Chen, Susan H.; Besser, Paul R.
PA Advanced Micro Devices, Inc., USA
SO U.S., 11 pp.
CODEN: USXXAM
DT Patent
LA English
IC ICM H01L021-28
NCL 438583000
CC 76-3 (Electric Phenomena)
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI US 6391750	B1	20020521	US 2000-639799	20000817
PRAI US 1999-149423P	P	19990818		

AB Methods are provided that selectively provide various contact resistances based on each individual **transistor**'s influence on an overall chip speed during the formation of **active regions** and silicide layers. In order to provide lower contact resistance to devices which have a crit. influence on overall device speed, the **active regions** of such crit. devices are formed with a lower dopant concn. and thicker silicide layers are provided on the **active regions**. Likewise, for the normal devices which have less or no influence on overall chip speed, thinner silicide layers are provided on the **active regions** having a higher dopant concn. than the crit. devices.

IT **7440-74-6**, Indium, uses
RL: **MOA (Modifier or additive use)**; USES (Uses)
(method of selectively controlling contact resistance of **transistors** by controlling dopant concn. and silicide thickness)
RN 7440-74-6 HCAPLUS
CN Indium (8CI, 9CI) (CA INDEX NAME)

In

L12 ANSWER 31 OF 49 HCAPLUS COPYRIGHT 2003 ACS on STN
AN 2002:221074 HCAPLUS
DN 136:255742
TI Advanced CMOS using super steep retrograde wells
IN Babcock, Jeffrey A.; Pinto, Angelo; Balster, Scott; Haeusler, Alfred; Howard, Gregory E.
PA Germany
SO U.S. Pat. Appl. Publ., 10 pp.
CODEN: USXXCO
DT Patent
LA English
IC ICM H01L031-119
ICS H01L031-113; H01L029-94
NCL 257408000
CC 76-3 (Electric Phenomena)
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI US 2002033511	A1	20020321	US 2001-948856	20010907
PRAI US 2000-232913P	P	20000915		

AB The present invention is a method for forming super steep doping profiles in MOS transistor structures. The method comprises forming a C contg. layer beneath the gate dielec. and source and drain regions of a MOS transistor. The C contg. layer will prevent the diffusion of dopants into the region directly beneath the gate **dielec. layer**.

IT **Dielectric films**
Doping
Epitaxial films
Ion implantation
IT **7440-74-6**, Indium, uses
RL: **MOA (Modifier or additive use)**; USES (Uses)
(advanced CMOS using super steep retrograde wells)
RN 7440-74-6 HCAPLUS
CN Indium (8CI, 9CI) (CA INDEX NAME)

In

No In doped dielec. over active

13/3,AB,K/1 (Item 1 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

01587052
DIPHENYLSQUARYLIUM COMPOUND AND DISPLAY FILTER CONTAINING THE SAME
DIPHENYLSQUARYLIUMVERBINDUNG SOWIE EIN DIESE ENTHALTENDES ANZEIGEELEMENT
COMPOSE DIPHENYLSQUARYLIUM ET FILTRE D'AFFICHAGE CONTENANT LEDIT COMPOSE
PATENT ASSIGNEE:
MITSUBISHI CHEMICAL CORPORATION, (1852041), 5-2 Marunouchi 2-chome, Chiyoda-ku, Tokyo 100-0005, (JP), (Applicant designated States: all)
INVENTOR:
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LEGAL REPRESENTATIVE:
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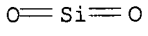
PATENT (CC, No, Kind, Date): EP 1316586 A1 030604 (Basic)
WO 2002020671 020314
APPLICATION (CC, No, Date): EP 2001961279 010831; WO 2001JP7565 010831
PRIORITY (CC, No, Date): JP 2000266415 000904; JP 2001104146 010403; JP 2001138101 010509
ABSTRACT EP 1316586 A1
The object of the invention is to provide a diphenylsquarylium compound which has a sharp minimum value within the wavelength range of from 550 to 610 nm in the light transmittance curve and from which a filter causing no reduction of brightness of the visual field can be obtained when used by containing in a filter for display, and a filter for display which contains this diphenylsquarylium compound.
Constructions of the invention are a diphenylsquarylium compound represented by the following general formula (I) and a filter for display which contains this diphenylsquarylium compound.

...SPECIFICATION aforementioned ones, a methine system compound other than the aforementioned ones and the like, and inorganic substances such as an antimony dope tin oxide, an **indium dope** tin oxide, and an oxide, carbide or boride of a metal belonging to the group IV, group V or group VI of the periodic table...

...thin film or dielectric substance layer having mesh-shaped pores and a metal layer alternately on a base material can also be used suitably. The **dielectric** substance layer includes **indium** oxide, zinc oxide and the like transparent metal oxides, and silver or a silver-palladium alloy is general as the metal layer. The laminate is...

L41 ANSWER 16 OF 77 HCAPLUS COPYRIGHT 2003 ACS on STN
AN 2001:465259 HCAPLUS
DN 135:217766
TI Preparation and optical properties of InAs0.4P0.6 nanocrystal alloy embedded in SiO2 thin films
AU Zheng, M. J.; Zhang, X. Y.; Yang, L.; Liang, C. H.; Zhang, L. D.
CS Institute of Solid State Physics, Chinese Academy of Sciences, Hefei, 230031, Peop. Rep. China
SO Semiconductor Science and Technology (2001), 16(6), 507-510
CODEN: SSTEET; ISSN: 0268-1242
PB Institute of Physics Publishing
DT Journal
LA English
CC 73-3 (Optical, Electron, and Mass Spectroscopy and Other Related Properties)
AB InAs0.4P0.6 nanocrystals with a size of 4.3-6.5 nm embedded in SiO2 thin films were prepd. by the radiofrequency magnetron co-sputtering technique. X-ray diffraction and Raman spectra strongly suggest the existence of InAs0.4P0.6 nanocrystals in SiO2 matrixes. The size distribution of the nanocrystals was obsd. by TEM. The optical transmission spectra indicate that the optical absorption band edge of the composite thin films can be modulated in a very large wavelength range by changing the prepn. conditions. The InAs0.4P0.6 nanocrystals exhibit the behavior of a direct bandgap. The marked blue shift of the optical absorption edge with respect to the bulk semiconductor can be explained by the quantum confinement effect.
IT **7631-86-9**, Silica, properties
RL: PRP (Properties)
(**indium** arsenide phosphide-**doped**; prepn. and optical properties of **indium** arsenide phosphide nanocrystal alloy embedded in silica thin films)
RN 7631-86-9 HCAPLUS
CN Silica (6CI, 7CI, 8CI, 9CI) (CA INDEX NAME)



L12 ANSWER 45 OF 49 HCAPLUS COPYRIGHT 2003 ACS on STN
AN 2000:688487 HCAPLUS
DN 133:274027
TI High efficiency electrodes for organic light emitting diode devices
IN Jones, Gary W.; Anandan, Munisamy
PA Fed Corporation, USA
SO PCT Int. Appl., 16 pp.
CODEN: PIXXD2
DT Patent
LA English
IC ICM H01J001-62
CC 73-11 (Optical, Electron, and Mass Spectroscopy and Other Related Properties)
Section cross-reference(s): 76
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	WO 2000057446	A1	20000928	WO 2000-US6929	20000317
PRAI	US 1999-125239P	P	19990319		

AB Org. light-emitting diodes comprising a substrate, a first conductor formed on the substrate, an org. stack formed on the first conductor, and a second conductor formed on the org. stack. are described in which .gtoreq.1 of the conductors comprise a thin layer of dielec. material and a conducting layer. The thin layer of dielec. material may include a doped dielec. material. The doped dielec. material may include between 5-50 % of a conducting material. The conducting material may include one of Mg, Ca, Ce, Ba, Al, Sn, Ga, and In. The thin layer of dielec. material may include one of lithium fluoride, cesium fluoride, and silicon monoxide. The conductor structures are also claimed. Methods for fabricating org. light-emitting diodes including the formation of the conducting structures are also described.
IT **7440-74-6**, Indium, uses
RL: DEV (Device component use); **MOA (Modifier or additive use)**; USES (Uses)
(electrodes comprising conductor layer/**dielec. layer** stacks for org. light-emitting devices and their fabrication)
RN 7440-74-6 HCAPLUS
CN Indium (8CI, 9CI) (CA INDEX NAME)

In

Active Region 7

L53 ANSWER 3 OF 9 HCAPLUS COPYRIGHT 2003 ACS on STN
AN 2001:823600 HCAPLUS
DN 135:338011
TI Partial formation of anti-short-channel **doped** area on the source side in MOS **transistor** fabrication
IN Wang, Jau-Jie; Tsai, Jau-Jie; Liou, Jing-Meng
PA Taiwan Semiconductor Manufacturing Co., Ltd., Taiwan
SO Taiwan, 16 pp.
CODEN: TWXXA5
DT Patent
LA Chinese
IC ICM H01L021-336
CC 76-3 (Electric Phenomena)
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	TW 381311	B	20000201	TW 1998-87112503	19980729
PRAI	TW 1998-87112503		19980729		

AB A MOS device is comprised of a semiconductor substrate sepd. from an **active area** by a spacer, a gate electrode formed in the **active area**, a channeling area with two ends under the gate electrode, a drain electrode of first cond.-type doped area formed in one end of the channel, a source electrode of first cond.-type on the other end of the channel with a dented area, a bulk contact area of second cond.-type doped area formed in the dented area of mentioned above, an anti-short-channel doped area of second cond.-type formed under the channel area close to the above drain electrode side as well as to the side of source electrode area except the bulk contact area. Therefore, a silicon substrate has an effective usage of the surface area and increased productivity.

IT **7440-74-6D**, Indium, ion, uses
RL: **MOA (Modifier or additive use)**; USES (Uses)
(ion implantation; partial formation of anti-short-channel doped area on source side in MOS **transistor** fabrication)
RN 7440-74-6 HCAPLUS
CN Indium (8CI, 9CI) (CA INDEX NAME)

In

L12 ANSWER 49 OF 49 HCAPLUS COPYRIGHT 2003 ACS on STN
AN 1999:427370 HCAPLUS
DN 131:81511
TI Nonvolatile semiconductor memory devices and erasing written-in signals
IN Fujiwara, Ichiro
PA Sony Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 12 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
IC ICM H01L021-8247
ICS H01L029-788; H01L029-792; G11C016-04; H01L027-115
CC 76-3 (Electric Phenomena)
Section cross-reference(s): 56, 57
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 11186421	A2	19990709	JP 1997-357914	19971225
PRAI	JP 1997-357914		19971225		

AB The gate insulator film bound below a gate electrode and above a channel region in the title devices comprises a thick upper insulator film, a thin tunnel insulator film, and conductive charging particles dispersed horizontally or spaciously on the tunnel insulator film. The conductive charging particles are amphoteric traps which may be charged with electron, hole, or neither of them in a neutral condition. The tunnel insulator film may be made from Si oxynitride at least on the side contacted by the conductive charging particles. The gate electrode may be made from a semiconductor with its cond. same as that of the channel region. The composite gate insulator gives an increased Vth shifting level for high-mobility read-out and low-voltage program driving without deterioration of data retention and write-in rate.

IT **7440-74-6**, Indium, properties
RL: DEV (Device component use); **MOA (Modifier or additive use)**; PEP (Physical, engineering or chemical process); PRP (Properties); TEM (Technical or engineered material use); PROC (Process); USES (Uses)
(conductive charging particles; nonvolatile semiconductor memory devices and erasing written-in signals)
RN 7440-74-6 HCAPLUS
CN Indium (8CI, 9CI) (CA INDEX NAME)

In

L41 ANSWER 12 OF 77 HCAPLUS COPYRIGHT 2003 ACS on STN
AN 2002:425488 HCAPLUS
DN 136:408832
TI Acoustooptical devices having thin film of silica and indium-containing material formed over optical waveguide
IN Seino, Minoru; Nakazawa, Tadao; Taniguchi, Shinji
PA Fujitsu Limited, Japan
SO U.S., 22 pp.
CODEN: USXXAM
DT Patent
LA English
IC ICM G02B006-00
ICS G02F001-335
NCL 385130000
CC 73-11 (Optical, Electron, and Mass Spectroscopy and Other Related Properties)
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 6400881	B1	20020604	US 1998-118936	19980720
JP 11064809	A2	19990305	JP 1997-216050	19970811

PRAI JP 1997-216050 A 19970811

AB Acoustooptical devices are described which comprise a substrate; an optical waveguide formed on the substrate to guide the light; a transducer formed on the substrate to excite a surface acoustic wave on the substrate and rotate the polarization state of the light; and a thin film formed of silicon dioxide and an indium-contg. material covering a portion of the optical waveguide; where the thin film is transparent to the light guided by the optical waveguide and has a refractive index < that of the optical waveguide, or where the speed of sound under the thin film is < that in a portion of the substrate not covered by the film. Acoustooptical devices are also described which comprise a substrate; a polarization beam splitter formed on the substrate and having input and output sides; a first pair of optical waveguides formed on the substrate to meet at the input side of the polarization beam splitter; a second pair of optical waveguides formed on the substrate to meet at the output side of the polarization beam splitter; a transducer formed on the substrate to excite a surface acoustic wave; and a thin film covering a portion of each waveguide of either the first or second pairs of optical waveguides, where the thin film is formed of silicon dioxide with an indium-contg. material added to it.

IT **Dielectric films**
IT **7631-86-9**, Silicon oxide (SiO2), uses
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PYP (Physical process); PROC (Process); USES (Uses)
(thin film; acoustooptical devices having thin film of silica and **indium**-contg. material formed over optical waveguide)
RN 7631-86-9 HCAPLUS
CN Silica (6CI, 7CI, 8CI, 9CI) (CA INDEX NAME)

O=Si=O

NO active core

NO

L12 ANSWER 40 OF 49 HCAPLUS COPYRIGHT 2003 ACS on STN
AN 2001:560106 HCAPLUS
DN 135:115642
TI Semiconductor devices with good stability and a flat insulating layer with a dopant
IN Watanabe, Hiroyuki; Mizuhara, Hideki; Misawa, Kaori; Hirase, Masaki; Aoe, Hiroyuki
PA Sanyo Electric Co., Ltd., Japan
SO U.S., 48 pp., Cont.-in-part of U.S. 6,214,479.
CODEN: USXXAM
DT Patent
LA English
IC ICM H01L021-321
ICS H01L023-485
NCL 257759000
CC 76-3 (Electric Phenomena)
FAN.CNT 4

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI US 6268657	B1	20010731	US 1997-877931	19970618
JP 09312339	A2	19971202	JP 1996-181593	19960620
JP 3015738	B2	20000306		
US 6214749	B1	20010410	US 1997-949283	19971021
US 6177343	B1	20010123	US 1999-429698	19991028
US 6326318	B1	20011204	US 2000-521865	20000308

AB A semiconductor device and a process for producing the same. The device has two conducting layers that are spaced from each other and an insulating film for elec. insulating these two conducting layers from each other. The insulating film contains contact holes with plugs being embedded therein so as to elec. connect these two conducting layers by the plugs. The process contains a step of forming the insulating film on the lower conducting layer. An impurity having a kinetic energy is introduced into the insulating film. Next, contact holes are formed in the insulating film, and then plugs are formed in the contact holes. An upper conducting layer is formed on the insulating film so as to be elec. connected to the plugs.

IT Contact holes
Dielectric films
Dopants
IT **7440-74-6**, Indium, uses
RL: **MOA (Modifier or additive use)**; USES (Uses)
(semiconductor devices with good stability and flat insulating layer with dopant)
RN 7440-74-6 HCAPLUS
CN Indium (8CI, 9CI) (CA INDEX NAME)

In

NO CONC'

13/3,AB,K/4 (Item 4 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00750769
Method for fabricating an integrated circuit
Verfahren zur Herstellung einer integrierten Schaltungsanordnung
Procede de fabrication d'un circuit integre
PATENT ASSIGNEE:
ADVANCED MICRO DEVICES INC., (328124), One AMD Place, P.O. Box 3453, Sunnyvale, California 94088-3453, (US), (Proprietor designated states: all)
INVENTOR:
Anjum, Mohammed, 10107 Jupiter Hills Drive, Austin, Texas 78747, (US)
Stuber, Alan, L., 2200 Crownspoint, Austin, Texas 78748, (US)
Burki, Ibrahim, K., 2208 Fancy Gap Lane, Austin, Texas 78745, (US)
LEGAL REPRESENTATIVE:
Picker, Madeline Margaret et al (78551), Brookes & Martin, High Holborn House, 52/54 High Holborn, London WC1V 6SE, (GB)
PATENT (CC, No, Kind, Date): EP 707345 A1 960417 (Basic)
EP 707345 B1 000105
APPLICATION (CC, No, Date): EP 95307087 951006;
PRIORITY (CC, No, Date): US 320924 941011

ABSTRACT EP 707345 A1

An MOS device is provided using indium as a threshold adjust implant in the channel regions of an NMOS device and/or in the conductive gate overlying the channel region in a PMOS device. **Indium ions** are relatively immobile and achieve location stability in the areas in which they are implanted. They do not readily segregate and diffuse in the lateral directions as well as in directions perpendicular to the silicon substrate. Placement immobility is necessary in order to minimize problems of threshold skew and gate oxide thickness enhancement. Additionally, it is believed that **indium atoms** within the channel region minimize hot carrier effects and the problems associated therewith.

...SPECIFICATION can be implanted into the channel region of an NMOS device to enhance the threshold of that device while minimizing the possibility of the larger **indium atoms** segregating and diffusing from their implanted positions. Specifically, the **indium atoms** have a lesser tendency to segregate and diffuse in a lateral direction toward the source/drain implanted areas. Moreover, **indium atoms** maintain their position and do not diffuse to a substantial degree to overlying gate oxide. Thus, indium provides a significant advantage over boron as a...

...less channeling due to pre-amorphization. Boron can be used as an impurity source for the source/drain regions provided the boron is implanted after **indium implantation**. Indium serves as a barrier in the polysilicon material by stuffing grain boundary locations. Therefore, while indium can be used as the only dopant within...

...deeper than boron.

An important advantage of indium is its larger atomic mass and the characteristic by which its implanted position is maintained. That is, **indium implanted** position is maintained within the active region, which includes the source/drain regions, the channel region (i.e., threshold adjust area), and the polysilicon gate...

...devices upon a single monolithic substrate. The method includes the steps of providing an opening to an active region of a semiconductor substrate upper surface. **Indium ions** can then be implanted through the opening and into the active regions, whereby a polysilicon gate material can then be deposited upon the active region...

...active region to complete the source/drain implant as well as polysilicon implant of a PMOS device.

In threshold adjust implant of an NMOS device, **indium ions** are preferably injected to a concentration peak density at a first depth relative to the semiconductor substrate upper surface. An insulating layer, preferrably a silicon dioxide in the gate region, is grown upon and into the silicon substrate active region to a depth limited by the first depth. The implanted **indium ions** can be injected either before or after the gate insulator is formed. If injected before gate **insulator** formation, then **indium** can be used as a growth-stop barrier of gate **insulator** (oxide) grown into the underlying silicon. **Indium** can therefore be used to closely control gate oxide growth and prevent unwanted continued growth during subsequent anneal cycles.

Implanted indium in the channel region...

...bonding between channel-region indium and source/drain region n-type implanted ions. N-type ions are generally large arsenic ions similar to the large **indium ions** and therefore do not easily migrate from their implanted positions. Leff is therefore maintained. Further, channel-implanted indium helps minimize problems of hot-electron effects ...

...indium suffices not only as the source/drain dopant, but also as large, substantially immobile dopants within polysilicon overlying the PMOS channel region. Somewhat immobile **indium ions** do not easily migrate from the polysilicon target areas to underlying channel regions and therefore do not cause OTE problems or threshold skews normally associated...

...the semiconductor substrate having localized field oxides formed according to the LOCOS process;

Fig. 3 is a cross-sectional view of the semiconductor substrate undergoing **indium implant** into a channel region according to the present invention;

Fig. 4 is a cross-sectional view along area 5 or 6 of Fig. 4 showing a semiconductor substrate active region having an **indium implant** region formed within the channel region beneath a gate oxide according to the present invention;

Fig. 5 is a cross-sectional view along area 5...

...subsequent to that shown in Fig. 3;

Fig. 5A is a detailed view along area 5A ofFig. 5 showing advantages at an atomic level of **indium implant** within the channel region;

Fig. 5B is a graph of concentration density versus depth of **indium implant** into the channel region of Fig. 3 according to the present invention;

Fig. 6 is a cross-sectional view along area 6 of Fig. 3 showing the semiconductor substrate active region of a PMOS device undergoing source/drain **indium implant** at a step subsequent to, or in lieu of, the implant shown in Fig. 3;

Fig. 6A is a cross-sectional view along area 6...Fig. 3, a step subsequent to that of Fig. 2 is shown in which indium is implanted into active regions 24. Fig. 3 illustrates exemplary **indium implantation** into both p-well 12 and n-well 14 active regions. However, it is understood by a skilled artisan that photoresist can be used and placed over n-well to achieve **indium implantation** only within p-well 12. The same can be true in the converse. **Indium implant** can be advantageously inserted into the bare upper surface 16 of substrate 10 or through a gate oxide formed in a step prior to **indium implant**. Thus, **indium implant** of Fig. 3 is used to adjust the thresholds of devices formed within active regions 24, wherein area 26 comprises a shallow **indium implant** or a gate

oxide adapted to receive an **indium implant**.

Indium is implanted using an ion implant device which ionizes elemental indium and accelerates the **indium ions** at an exemplary dose within the range of 1 x 1012) atoms/cm2) to 1 x 1013) atoms/cm2). Advantageously, the ion implant device can...

...shallow threshold adjust in active regions 24 is necessary when channel lengths are quite small, and preferably in the range of three microns or less.

Indium implant into active region 26 of p-well 12 will increase the thresholds of the ensuing NMOS device. Conversely, **indium implant** into active region 26 of n-well 14 will decrease the threshold of the ensuing PMOS device.

Referring to Fig. 4, active regions 24 of areas 5 or 6 is shown. In particular, Fig. 4 aids in describing the formation of area 26. Area 26 includes **indium implant** 28 beneath gate oxide 30. Indium region 28 is formed either before gate oxide 30 is grown or after gate oxide 30. Indium region 28...

...that oxygen atoms of gate oxide 30 bond with silicon atoms at upper surface 16. If silicon atoms are bonded with a predominate amount of **indium atoms**, then there remains insufficient number of bond locations in which oxygen can occupy thereby limiting the downward growth of oxide 30. **Indium implant** region 28 therefore suffices as a mechanism for closely controlling the thickness of gate oxide 30 -- an advantageous outcome for achieving close control of device...

...type ions, either arsenic (As) or phosphorous (P).

Source/drain implantation of Fig. 5 occurs at a step subsequent to that of Fig. 3, wherein **indium ions** are predisposed within active region 24 and, specifically, within channel area 36 underlying conductive gate 32 and gate oxide 30. **Indium implant** region 28 is therefore formed within channel region 36, between source/drain regions 34. The NMOS structure of Fig. 5 is formed using the lightly...

...Fig. 5A, a detailed view along area 5A of Fig. 5 is provided and shown at an atomic level. Fig. 5A illustrates the threshold adjust **indium implant** region 28 having **indium atoms** 42 placed therein. **Indium atoms** 42 maintain their implanted position despite subsequent high temperature thermal cycles inherent in semiconductor fabrication. **Indium atoms** 42, due to their large atomic mass, have difficulty moving through the silicon lattice to adjacent (lateral or overlying) positions. For example, Fig. 5A illustrates **indium atom** 42a moving only slightly toward adjacent lightly doped source/drain regions 40, as indicated by destination location 42b. Likewise, implanted **indium atoms** 42a near the lower surface of gate oxide 30 move only slightly toward gate oxide 30 to destination location 42b. Relative attachment at the implant...

...Any OTE or lateral diffusion can limit the effectiveness of the threshold adjust by lowering the threshold value.

Fig. 5A further describes the advantages of **indium implant** as a deterrent against hot carrier effects. Specifically, the large atomic mass and size of indium limits impact ionization of electrons which become hot near...smaller atomic units within the channel to cause dislodgement of holes traveling in the reverse direction. It is postulated that, as a result of larger **indium atoms**, carriers in the channel cannot obtain sufficient energy to be termed "hot" carriers since they are scattered by the larger **indium atoms**. Scattering lowers the carrier energy thereby reducing hot carrier (or hot electron) effects normally associated with NMOS devices. In addition, larger **indium atoms** minimizes injection of electrons (shown by reference numeral 48) into gate oxide 30 from a drain region 40. Minimization of hot carrier injection into gate...

...in impact ionization helps minimize or reduce the problems of hot carrier effects.

Referring to Fig. 5B, a graph of concentration density versus depth of **indium implant** into channel region 36 is shown. Target **indium implant** is to a concentration peak density at a depth just below the lower surface of gate oxide 30. Concentration peak density is shown at a...

...of substrate 10 or beneath the initial lower surface of gate oxide 30, depending upon the relative order of gate oxide growth with respect of **indium implant**.

Turning now to Fig. 6, a cross-sectional view along area 6 of Fig. 3 is shown at a step subsequent to that of Fig. 3. Specifically, Fig. 6 illustrates active region 24 of a PMOS device undergoing source/drain **indium implant**. Indium is implanted not only in source/drain regions 34 to form the p-type impurity therein, but also to a specified depth relative to...

...drain implant instead of boron or boron difluoride allows a more controlled, shallower implant at the source/drains when using high energy implant devices. Once **indium implant** is achieved, as shown in Fig. 6, subsequent metallization can be coupled to the source/drain junctions to complete the circuit interconnect structure without requiring...

...36. It is appreciated that boron need not be used as the source/drain implant material, however, if it is used, it is used after **indium implant**. The larger **indium atoms** sufficiently "stuff" grain boundary locations as well as the grains themselves of polycrystalline silicon conductive gate 32 and prevent interstitial and substitutional movements of overlying...

...graph of Fig. 6B illustrates various concentration densities of implanted p-type ions (indium and boron) into conductive gate 32 and above gate oxide 30. **Indium ions** are shown implanted at a concentration peak density at a first depth above gate oxide 30 as well as channel region 36. P-type ions...

...at D2)). Indium species can be implanted to a depth sufficient to prevent what is commonly referred to as the "depletion effect". After thermal cycles, **indium atoms** extend substantially across the polysilicon profile to minimize unwanted gate capacitance attributed to active boron or unwanted impurities subsequently placed in the polysilicon.

It will...

13/3,AB,K/7 (Item 7 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00657879
PATENT ASSIGNEE:
STMicroelectronics, Inc., (723064), 1310 Electronics Drive, Carrollton, TX 75006-5039, (US), (applicant designated states: DE;FR;GB;IT)
PATENT (CC, No, Kind, Date): EP 632492 A3 961120 (Basic)

ABSTRACT EP 632492 A3
A prior art thin film transistor structure having a first and a second polycrystalline silicon layer of different conductivity types (P and N) has a high resistance contact at the resultant P-N junction. This contact resistance is reduced by forming TiSi(sub(2)) (titanium disilicide) or other refractory metal silicides such as cobalt or molybdenum in specific regions, namely the P-N junction contact. Titanium disilicide consumes the portion of the second polycrystalline silicon layer in the P-N contact junction and at the same time consumes a small portion of the underlying first polycrystalline silicon layer, such that the high resistance P-N junction now no longer exists.
The procedure to form low resistance contacts is extended to achieve a low leakage polysilicon TFT device. One or more LDD regions are formed to reduce the amount of leakage current of such transistor devices in an "OFF" state. The source/drain region(s) of the device are implanted with a first dopant type followed by an etch which forms spacers above the source/drain regions. Then, the source/drain regions are implanted with a second dopant type so that LDD regions are formed beneath the spacers. The electric field at the gate and source/drain boundaries of the device is spread over the entire LDD region, resulting in a lower peak electric field and hence less device leakage current. (see image in original

...SPECIFICATION a P(sup +) dopant material and patterning and etching the second polycrystalline silicon layer.
Preferably the implant steps may be performed with Boron, BF2 or **Indium dopant** material.,
Preferably the **insulating** layer is implanted with a P(sup -)(sup -) dosage of approximately 1 x 10(sup 1)(sup 6) per cm(sup 3).
Preferably the source...a P(sup +) dopant material and patterning and etching the second polycrystalline silicon layer.
Preferably the implant steps may be performed with Boron, BF2 or **Indium dopant** material.
Preferably the **insulating** layer is implanted with a P(sup -) dosage of approximately 1 x 10(sup 1)(sup 7) per cm(sup 3).
Preferably the source/drain...

...a P(sup +) dopant material, and patterning and etching the second polycrystalline silicon layer.
Preferably the implant steps may be performed with Boron, BF2 or **Indium dopant** material.
Preferably the source/drain regions of the insulating layer are implanted with a P(sup -) dosage of approximately 1 x 10(sup 1)(sup...

13/3,AB,K/3 (Item 3 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00750770
Method for fabricating an integrated circuit
Verfahren zur Herstellung einer integrierten Schaltungsanordnung
Procede de fabrication d'un circuit integre
PATENT ASSIGNEE:
ADVANCED MICRO DEVICES INC., (328124), One AMD Place, P.O. Box 3453,
INVENTOR:
Anjum, Mohammed, 10107 Jupiter Hills Drive, Austin, Texas 78747, (US)
Stuber, Alan L., 2200 Crownspoint, Austin, Texas 78748, (US)
PATENT (CC, No, Kind, Date): EP 707346 A1 960417 (Basic)
APPLICATION (CC, No, Date): EP 95307088 951006;
PRIORITY (CC, No, Date): US 320897 941011
ABSTRACT EP 707346 A1
An MOS device is provided using indium as a threshold adjust implant in the channel regions of an NMOS device and/or in the conductive gate overlying the channel region in a PMOS device. **Indium ions** are relatively immobile and achieve location stability in the areas in which they are implanted. They do not readily segregate and diffuse in the lateral directions as well as in directions perpendicular to the silicon substrate. Placement immobility is necessary in order to minimize problems of threshold skew and gate oxide thickness enhancement. Additionally, it is believed that **indium atoms** within the channel region minimize hot carrier effects and the problems associated therewith.

No core.

...SPECIFICATION can be implanted into the channel region of an NMOS device to enhance the threshold of that device while minimizing the possibility of the larger **indium atoms** segregating and diffusing from their implanted positions. Specifically, the **indium atoms** have a lesser tendency to segregate and diffuse in a lateral direction toward the source/drain implanted areas. Moreover, **indium atoms** maintain their position and do not diffuse to a substantial degree to overlying gate oxide. Thus, indium provides a significant advantage over boron as a...not necessary for the present invention, boron can be used as an impurity source for the source/drain regions provided the boron is implanted after **indium implantation**. Indium serves as a barrier in the polysilicon material by stuffing grain boundary locations. Therefore, while indium is preferred as the only dopant within the...

...deeper than boron.
An important advantage of indium is its larger atomic mass and the characteristic by which its implanted position is maintained. That is, **indium implanted** position is maintained within the active region, which includes the source/drain regions, the channel region (i.e., threshold adjust area), and the polysilicon gate...
...devices upon a single monolithic substrate. The method includes the steps of providing an opening to an active region of a semiconductor substrate upper surface. **Indium ions** can then be implanted through the opening and into the active regions, whereby a polysilicon gate material can then be deposited upon the active region...

...active region to complete the source/drain implant as well as polysilicon implant of a PMOS device.
In threshold adjust implant of an NMOS device, **indium ions** are preferably injected to a concentration peak density at a first depth relative to the semiconductor substrate upper surface. An insulating layer, preferrably a silicon dioxide in the gate region, is grown upon and into the silicon substrate active region to a depth limited by the first depth. The implanted **indium ions** can be injected either before or after the gate insulator is formed. If injected before

gate **insulator** formation, then **indium** can be used as a growth-stop barrier of gate **insulator** (oxide) grown into the underlying silicon. **Indium** can therefore be used to closely control gate oxide growth and prevent unwanted continued growth during subsequent anneal cycles.

Implanted indium in the channel region...

...bonding between channel-region indium and source/drain region n-type implanted ions. N-type ions are generally large arsenic ions similar to the large **indium ions** and therefore do not easily migrate from their implanted positions. Leff is therefore maintained. Further, channel-implanted indium helps minimize problems of hot-electron effects ...

...indium suffices not only as the source/drain dopant, but also as large, substantially immobile dopants within polysilicon overlying the PMOS channel region. Somewhat immobile **indium ions** do not easily migrate from the polysilicon target areas to underlying channel regions and therefore do not cause OTE problems or threshold skews normally associated...

...the semiconductor substrate having localized field oxides formed according to the LOCOS process;

Fig. 3 is a cross-sectional view of the semiconductor substrate undergoing **indium implant** into a channel region ...present invention;

Fig. 4 is a cross-sectional view along area 5 or 6 of Fig. 4 showing a semiconductor substrate active region having an **indium implant** region formed within the channel region beneath a gate oxide according to the present invention;

Fig. 5 is a cross-sectional view along area 5...

...to that shown in Fig. 3;

Fig. 5A is a detailed view along area 5A of Fig. 5 showing advantages at an atomic level of **indium implant** within the channel region;

Fig. 5B is a graph of concentration density versus depth of **indium implant** into the channel region of Fig. 3 according to the present invention;

Fig. 6 is a cross-sectional view along area 6 of Fig. 3 showing the semiconductor substrate active region of a PMOS device undergoing source/drain **indium implant** at a step subsequent to, or in lieu of, the implant shown in Fig. 3;

Fig. 6A is a cross-sectional view along area 6...

...Fig. 3, a step subsequent to that of Fig. 2 is shown in which indium is implanted into active regions 24. Fig. 3 illustrates exemplary **indium implantation** into both p-well 12 and n-well 14 active regions. However, it is understood by a skilled artisan that photoresist can be used and placed over n-well to achieve **indium implantation** only within p-well 12. The same can be true in the converse. **Indium implant** can be advantageously inserted into the bare upper surface 16 of substrate 10 or through a gate oxide formed in a step prior to **indium implant**. Thus, **indium implant** of Fig. 3 is used to adjust the thresholds of devices formed within active regions 24, wherein area 26 comprises a shallow **indium implant** or a gate oxide adapted to receive an **indium implant.**

Indium is implanted using an ion implant device which ionizes elemental indium and accelerates the **indium ions** at an exemplary dose within the range of 1 x 10(sup 1)(sup 2) atoms/cm(sup 2) to 1 x 10(sup 1 necessary when channel lengths are quite small, and preferably in the range of three microns or less.

Indium implant into active region 26 of p-well 12 will increase the thresholds of the ensuing NMOS device. Conversely, **indium implant** into active region 26 of n-well 14 will

decrease the threshold of the ensuing PMOS device.

Referring to Fig. 4, active regions 24 of areas 5 or 6 is shown. In particular, Fig. 4 aids in describing the formation of area 26. Area 26 includes **indium implant** 28 beneath gate oxide 30. Indium region 28 is formed either before gate oxide 30 is grown or after gate oxide 30. Indium region 28...

...that oxygen atoms of gate oxide 30 bond with silicon atoms at upper surface 16. If silicon atoms are bonded with a predominate amount of **indium atoms**, then there remains insufficient number of bond locations in which oxygen can occupy thereby limiting the downward growth of oxide 30. **Indium implant** region 28 therefore suffices as a mechanism for closely controlling the thickness of gate oxide 30 -- an advantageous outcome for achieving close control of device...

...type ions, either arsenic (As) or phosphorous (P).

Source/drain implantation of Fig. 5 occurs at a step subsequent to that of Fig. 3, wherein **indium ions** are predisposed within active region 24 and, specifically, within channel area 36 underlying conductive gate 32 and gate oxide 30. **Indium implant** region 28 is therefore formed within channel region 36, between source/drain regions 34. The NMOS structure of Fig. 5 is formed using the lightly...

...Fig. 5A, a detailed view along area 5A of Fig. 5 is provided and shown at an atomic level. Fig. 5A illustrates the threshold adjust **indium implant** region 28 having **indium atoms** 42 placed therein. **Indium atoms** 42 maintain their implanted position despite subsequent high temperature thermal cycles inherent in semiconductor fabrication. **Indium atoms** 42, due to their large atomic mass, have difficulty moving through the silicon lattice to adjacent (lateral or overlying) positions. For example, Fig. 5A illustrates **indium atom** 42a moving only slightly toward adjacent lightly doped source/drain regions 40, as indicated by destination location 42b. Likewise, implanted **indium atoms** 42a near the lower surface of gate oxide 30 move only slightly toward gate oxide 30 to destination location 42b. Relative attachment at the implant...

...Any OTE or lateral diffusion can limit the effectiveness of the threshold adjust by lowering the threshold value.

Fig. 5A further describes the advantages of **indium implant** as a deterrent against hot carrier effects. Specifically, the large atomic mass and size of indium limits impact ionization of electrons which become hot near...

...smaller atomic units within the channel to cause dislodgement of holes traveling in the reverse direction. It is postulated that, as a result of larger **indium atoms**, carriers in the channel cannot obtain sufficient energy to be termed "hot" carriers since they are scattered by the larger **indium atoms**. Scattering lowers the carrier energy thereby reducing hot carrier (or hot electron) effects normally associated with NMOS devices. In addition, larger **indium atoms** minimizes injection of electrons (shown by reference numeral 48) into gate oxide 30 from a drain region 40. Minimization of hot carrier injection into gate...

...in impact ionization helps minimize or reduce the problems of hot carrier effects.

Referring to Fig. 5B, a graph of concentration density versus depth of **indium implant** into channel region 36 is shown. Target **indium implant** is to a concentration peak density at a depth just below the lower surface of gate oxide 30. Concentration peak density is shown at a...

...of substrate 10 or beneath the initial lower surface of gate oxide 30,

depending upon the relative order of gate oxide growth with respect of **indium implant**.

Turning now to Fig. 6, a cross-sectional view along area 6 of Fig. 3 is shown at a step subsequent to that of Fig. 3. Specifically, Fig. 6 illustrates active region 24 of a PMOS device undergoing source/drain **indium implant**. Indium is implanted not only in source/drain regions 34 to form the p-type impurity therein, but also to a specified depth relative to...drain implant instead of boron or boron difluoride allows a more controlled, shallower implant at the source/drains when using high energy implant devices. Once **indium implant** is achieved, as shown in Fig. 6, subsequent metallization can be coupled to the source/drain junctions to complete the circuit interconnect structure without requiring...

...36. It is appreciated that boron need not be used as the source/drain implant material, however, if it is used, it is used after **indium implant**. The larger **indium atoms** sufficiently "stuff" grain boundary locations as well as the grains themselves of polycrystalline silicon conductive gate 32 and prevent interstitial and substitutional movements of overlying...

...graph of Fig. 6B illustrates various concentration densities of implanted p-type ions (indium and boron) into conductive gate 32 and above gate oxide 30. **Indium ions** are shown implanted at a concentration peak density at a first depth above gate oxide 30 as well as channel region 36. P-type ions...

...sub 2). Indium species can be implanted to a depth sufficient to prevent what is commonly referred to as the "depletion effect". After thermal cycles, **indium atoms** extend substantially across the polysilicon profile to minimize unwanted gate capacitance attributed to active boron or unwanted impurities subsequently placed in the polysilicon.

It will...

...CLAIMS A1

1. A method for fabricating an integrated circuit, comprising:
providing an opening to an active region of a semiconductor substrate upper surface;
implanting **indium ions** through said opening and into said active region; and
depositing a polysilicon gate material upon said active region.
2. The method as recited in claim 1, wherein said implanting step comprises:
injecting **indium ions** to a concentration peak density at a first depth relative to the semiconductor substrate upper surface; and
growing an insulating layer upon said active region...

...the semiconductor substrate consisting essentially of silicon.

8. The method as recited in claim 1, further comprising applying heat after said depositing step, wherein said **indium ions** implanted into said active region remain substantially within said active region during application of heat.
9. The method as recited in claim 1, after said...

...form an opening to source and drain regions within said active region;

implanting n-type ions into said source and drain regions adjacent the implanted **indium ions**; and
applying heat to anneal said source and drain region, wherein **indium ions** and said n-type ions, during application of heat, are substantially prevented from intermingling in bond locations with each other.

10. The method as recited...

L41 ANSWER 27 OF 77 HCAPLUS COPYRIGHT 2003 ACS on STN
AN 1998:37886 HCAPLUS
DN 128:135001
TI Theoretical analysis of kink effect in C-V characteristics of indium-implanted NMOS capacitors
AU Bouillon, P.; Skotnicki, T.
CS Department of Microelectronics, France Telecom, Centre national d'Etudes des Telecommunications, Meylan, 38243, Fr.
SO IEEE Electron Device Letters (1998), 19(1), 19-22
CODEN: EDLEDZ; ISSN: 0741-3106
PB Institute of Electrical and Electronics Engineers
DT Journal
LA English
CC 76-3 (Electric Phenomena)
AB Exptl. observation of an anomalous "kink" effect in C-V characteristics of **Indium-doped** NMOS capacitors is reported and explained, for the first time, via the impact of incomplete ionization of Indium. A new anal. formulation of the total semiconductor capacitance is developed, that takes incomplete ionization phenomenon into account. Thanks to this new Csc(.psi.s) relation, we have demonstrated that the carrier freeze-out is responsible for this kink near VFB in C-V curves, and also for an intrinsic lowering in the threshold voltage. This kink has been shown to be very sensitive to Indium dose and temp. It is also demonstrated that the deformation of the C-V characteristics due to Indium incomplete ionization may be (and probably has often been) miss-interpreted as appearance of high fixed charge densities in parameter extn. from C-V fitting.
IT **7631-86-9**, Silica, uses
RL: DEV (Device component use); USES (Uses)
(theor. anal. of kink effect in C-V characteristics of **indium**-implanted NMOS capacitors)
RN 7631-86-9 HCAPLUS
CN Silica (6CI, 7CI, 8CI, 9CI) (CA INDEX NAME)

O=Si=O

IT **7440-74-6**, Indium, uses
RL: **MOA (Modifier or additive use)**; USES (Uses)
(theor. anal. of kink effect in C-V characteristics of indium-**implanted** NMOS capacitors)
RN 7440-74-6 HCAPLUS
CN Indium (8CI, 9CI) (CA INDEX NAME)

In